CLAIMS

I CLAIM:

	1.	1. A method of positioning the active edge of a clock signal within the unit interval of a d			
4		the method comprising the steps of:			
	(a)		measuring in terms of a ΔT the unit interval of the data signal by:		
6			(a1)	applying the data signal to a delay line having taps ΔT apart, the overall delay of	
				the delay line being at least as long as the unit interval;	
8		-	(a2)	latching the logical values appearing at consecutive taps $2\Delta T$ apart upon a	
				transition in the logical value of the data signal;	
10			(a3)	generating a measured unit interval signal indicating the length of the unit interval	
				in terms of the number of consecutive latches having the same logical value latched	
12				in step (a2);	
		(b)	delay	ing a clock signal in units of ΔT and by a selected amount;	
14		(c)	measuring in terms of ΔT where in the unit interval the delayed clock signal of step (b)		
			exerts	s an active edge by:	
16		•	(c1)	applying the data signal to a delay line having taps ΔT apart;	
			(c2)	latching the logical values appearing at consecutive taps ΔT apart upon the active	
18				edge of the delayed clock signal;	
	,		(c3)	generating a clock phase signal indicating, in terms of a number of consecutive	
20				latches, where in the unit interval a transition occurred in the logical values	
				latched in step (c2);	
22		(d)	d) determining the selected amount of delay of step (b) according to the values of the		
			measi	ured unit interval signal of step (a3) and of the clock phase signal of step (c3).	
	2.	A method as in claim 1 wherein step (d) comprises the step shifting the value of the clock phase			
2		signal by an amount and in a direction determined by the value of the measured unit interval signal.			
	3.	A method as in claim 1 further comprising the step of using the same delay line for steps (a) and			
2		(c).			

4. A method as in claim 1 further comprising the steps of providing the delay line of step (a1) with an initial delay of a first amount that is larger than ΔT and of providing the delay line of step (c1) with an initial delay of a second amount that is larger than ΔT but less than the first amount.

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